PATENT
(5681-03600/P6750)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/007,816
Filed: November 9, 2001
Inventor(s):
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Steven A. Sivier
James P. Freyensee
Carl Cavanagh

Title: Message Packet Logging in a Distributed Simulation System

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Examiner: Silver, David
Group/Art Unit: 2128
Atty. Dkt. No: 5681-03600

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Lawrence J. Merkel
Name of Registered Representative

Signature 10/13/05 Date

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant requests consideration of ☒ the references listed on the attached Form PTO-1449 and/or ☐ the additional information identified below in paragraph 3.

1. This Information Disclosure Statement is submitted:

a. ☐ within 3 months of the filing date of a national application other than a continued prosecution application under § 1.53(d);
☐ within 3 months of the date of entry of the national stage as set forth in § 1.491 in an International application;
☐ before the mailing date of a first Office Action on the merits; or
☐ before the mailing of a first Office Action after the filing of a request for continued examination under § 1.114.

b. ☒ after the events of above paragraph 1a and prior to the mailing date of a final Office Action or Notice of Allowance, and thus: ☐ the certification of paragraph 2 below is provided, or ☒ a fee of $180.00 is enclosed.

c. ☐ after the mailing date of a final Office Action or a Notice of Allowance and prior to payment of the issue fee, and thus: the certification of paragraph 2 below is provided and a fee of $180.00 is enclosed.

2. It is hereby certified:

☐ that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the Statement, or

☐ that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing the certification after making reasonable inquiry, was known to any individual designated in § 1.56 (c) more than three months prior to the filing of the Statement.

3. ☐ Consideration of the following additional information (including any co-pending or abandoned U.S. applications, prior uses and/or sales, etc.) is requested:

4. For each non-English language reference listed on the attached Form PTO-1449:

☐ reference is made to an English language translation submitted herewith, and/or

☐ reference is made to a foreign patent office search report (in the English language) submitted herewith, and/or

☐ reference is made to an English language translation of a foreign patent office search report submitted herewith, and/or

☐ reference is made to the concise explanation contained in the specification of the present application at page(s) _____, and/or

☐ reference is made to the concise explanation set forth below:

5. ☐ Applicant also offers the following comments for the Examiner's consideration:

6. ☐ Also enclosed is a copy of a foreign search report citing these references.

7. ☐ The listed documents were brought to the attention of the Applicant(s) after payment of the issue fee in the captioned case. The documents were cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. Applicant(s) request this Information Disclosure Statement and attached Form PTO-1449 be placed in the file of the captioned application.

8. ☐ Applicant(s) requests that the Information Disclosure Statement and attached Form PTO-1449 and references, which are being filed before the grant of the patent and pursuant to 37 C.F.R. § 1.97(i), be placed in the file of the captioned application.

If any required fees are missing, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel, P.C. Deposit Account No. 50-1505/5681-03600/LJM.

Respectfully submitted,

Lawrence J. Merkel
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Date: 10/13/05

Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5681-03600 APPLICANT: Frankel, et al. FILING DATE: November 9, 2001	SERIAL NO. 10/007,816 GROUP: 2151

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	D1	Lee, K.C., "A Virtual Bus Architecture for Dynamic Parallel Processing Parallel and Distributed Systems," IEEE Transactions, Vol. 4, Issue 2, February 1993, pages 121-130.
	D2	Lee, K.C., "A Virtual Bus for Dynamic Parallel Processing Parallel and Distributed Processing, 1990, Proceedings of the Second IEEE Symposium on December 9-13, 1990, pages 736-743.
	D3	"Rule Base Driven Conversion of an Object Oriented Design Structure Into Standard Hardware Description Languages," Verschueren, A.C., IEEE Xplore, appears in Euromicro Conference, 1998, Proceedings. 24th, vol. 1, August 25, 1998, pages 42-45.
	D4	"Modeling Communication with Objective VHDL," Putzke, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 83-89.
	D5	"A Procedural Language Interface for VHDL and its Typical Applications," Martinolle, et al., IEEE Xplore, appears in Verilog HDL Conference and VHDL International Use Forum, 1998, IVC/VIUF, Proceedings., 1998 International, March 16, 1998, pages 32-38.
	D6	"The Verilog Procedural Interface for the Verilog Hardware Description Language," Dawson, et al., IEEE Xplore, appears in Verilog HDL Conference, 1996, Proceedings., 1996 International, February 26, 1996, pages 17-23.
	D7	"An Integrated Environment for HDL Verification," York, et al., IEEE Xplore, appears in Verilog HDL Conference, 1995, Proceedings., 1995 International, March 27, 1995, pages 9-18.
	D8	"The PowerPC 603 C++ Verilog Interface Model," Voith, R.P., IEEE Xplore, appears in Compcon Spring '94, Digest of Papters, Feb. 28, 1994, pages 337-340.
	D9	"Networked Object Oriented Verification with C++ and Verilog, Dearth, et al., IEEE, XP-002144328, 1998, 4 pages.
	D10	Patent Abstracts of Japan, publication no. 10326835, published December 8, 1998.
	D11	Patent Abstracts of Japan, publication no. 10049560, published February 20, 1998.
	D12	Patent Abstracts of Japan, publication no. 10340283, published December 22, 1998.
	D13	Patent Abstracts of Japan, publication no. 07254008, published October 3, 1995.
	D14	"Multiprocessing Verilog Simulator Exploits the Parallel Nature of HDLs." Lisa Maliniak, Electronic Design, Abstract, May 30, 1994, 1 page.

EXAMINER: DATE CONSIDERED:

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)		
	D15	"It's A Multithreaded World, Part I," Charles J. Northrup, BYTE, May 1992, 7 pages.
	D16	"It's a Multithreaded World, Part 2," Charles J. Northrup, BYTE, June 1992, pp. 351-356.
	D17	"Weaving a Thread," Shashi Prasad, BYTE, October 1995, pp. 173-174.
	D18	"Making Sense of Collaborative Computing," Mark Gibbs, Network World Collaboration, January 10, 1994, 4 pages.
	D19	"Parallel Logic Simulation of VLSI Systems," Bailey, et al., ACM Computing Surveys, Vol. 26, No. 3, September 1994, pp. 255-294.
	D20	"Multithreaded Languages for Scientific and Technical Computing," Cherri M. Pancake, Proceedings of the IEEE, Vol. 81, No. 2, February 1993, pp. 288-304.
	D21	"Distributed Simulation Architecture, SW Environment, Enterprise Server Products," Purdue EE400 Presentation by Freyensee and Frankel, November 9, 2000, 13 pages.
	D22	"BNF and EBNF: What Are They And How Do They Work?," Lars Marius Garshol, October 12, 1999, pp. 1-10.
	D23	"VCK: Verilog-C Kernel," Testbench Automation, Distributed by Verilog Simulation, Hardware-Software Co-verification, 2001 Avery Design Systems, Inc., 8 pages.
	D24	"Principles of Verilog PLI," Swapnajit Mittra, Silicon Graphics Incorporated, 1999, 10 pages.
	D25	"IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language," IEEE, December 12, 1995, 8 pages.
	D26	"OpenVera 1.0, Language Reference Manual," Version 1.0, March 2001, pp. 4-1 to 4-34, pp. 5-1 to 5-32, 6-1 to 6-22, 7-1 to 7-24, 11-1 to 11-50, 12-1 to 12-8, 13-1 to 13-14, 14-1 to 14-20, 15-1 to 15-118.
	D27	"VLSI Designe of a Bust Arbitration Module for the 68000 Series of Microprocessors," Ososanya, et al., IEEE, 1994, pp. 398-402.
	D28	"A VHDL Standard Package for Logic Modeling," David R. Coelho, IEEE Design & Test of Computers, Vol. 7, Issue 3, June 1990, pp. 25-32
	D29	"Corrected Settling Time of the Distributed Parallel Arbiter," M.M. Taub, PhD., IEEE Proceedings, Part E: Computers & Digitals, Vol. 139, Issue 4, July 1992, pp. 348-354.

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